

REMARKS

II. Response to Office Action

A. Status of the Pending Application

Claims 1-9 and 11-23 are pending in the application. Claims 1, 3, 9, 13, 15, and 21 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Chien et al. (U.S. Patent No. 6,319,839). Claims 2, 4, 14, and 16 stand rejected under § 103(a) as unpatentable over Chien et al. in view of Tseng (U.S. Patent No. 6,258,682). Claims 5-8, 11-12, 17-20, and 22-23 are objected to as being dependent upon a rejected base claim.

B. Prior Art Rejections

Claims 1, 3, 9, 13, 15, and 21 are not anticipated by Chien et al. (U.S. Patent No. 6,319,839)

Claims 1 and 13 recite, among other features, forming a gate insulation layer having a gate deposition-inhibiting layer, a gate layer and a covering deposition-inhibiting layer on a semiconductor substrate; patterning the gate layer and the covering deposition-inhibiting layer in order form gate stacks; and depositing an insulation layer selectively with respect to the deposition-inhibiting layers to form the spacer structure.

Chien et al. discloses a method for forming an inter-poly oxide (IPO) film between two polysilicon layers. The Examiner alleges that Chien et al. discloses the features of claims 1 and 13, including a gate insulation layer having a gate deposition inhibiting layer, a gate layer and a covering deposition-inhibiting layer on a semiconductor substrate (Office Action mailed March 31, 2006, at 2-3). The Examiner refers to Fig. 4 of Chien et al. where a polysilicon layer (13), an ONO layer (11), (12), (111), a silicon substrate (10) and a densified TEOS layer (44) are illustrated (See Chien et al., at Col. 3, ll. 8-20, and Fig. 4).

Chien et al., however, fails to disclose the covering deposition-inhibiting layer recited in claims 1 and 13. Chien et al. discloses an insulation layer, the TEOS layer

(44) shown in Fig. 4, but fails to disclose or suggest an oxynitride or nitride covering deposition-inhibiting layer as required by claims 1 and 13.

In addition, the Examiner asserts that it would be obvious to one of ordinary skill in the art to select a different range of an insulation layer 60 to form a spacer structure (Office Action mailed March 31, 2006, at 3). Selective deposition results in a high oxide growth established at the side walls of the gate stacks, while only slight oxide growth is observed at the horizontal surface of the deposition-inhibiting layers (See specification at p. 7, ll. 8-15). Selective deposition is not achieved, as suggested by the Examiner, by just selecting a different range of an insulation layer on the side walls. Selective deposition requires a specific process technology related to the deposited process layers. The Examiner is respectfully requested to provide a reference disclosing or suggesting "depositing an insulation layer selectively with respect to the deposition-inhibiting layers to form the spacer structure" as recited in claims 1 and 13. M.P.E.P. § 2144.03(A) (8th Ed. 2005) ("[A]ssertions of technical facts in the areas of esoteric technology or specific knowledge of the prior art must always be supported by citation to some reference work recognized as standard in the pertinent art." *In re Ahlert*, 424 F.2d at 1091, 165 USPQ at 420-21).

For all of these reasons, claims 1, 13, and claims 2-9, 11-12 and 14-23 depending therefrom, should be allowed over Chien et al, and notice to that effect is earnestly solicited.

C. Allowable Subject Matter

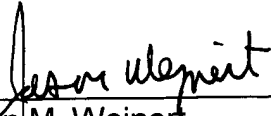
Applicant gratefully acknowledges that the Examiner has indicated claims 5-8, 11-12, 17-20 and 22-23 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

D. SUMMARY

Pending Claims 1-9 and 11-23 are patentable. Applicant respectfully requests the Examiner grant early allowance of this application. The Examiner is

invited to contact the undersigned attorney for the Applicant via telephone if such communication would expedite this application.

Respectfully submitted,



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